REMARKS

Claims 1-29 and 33-37 are pending in the application. No claims have been amended. Claims 30-32 have been cancelled and claims 36 and 37 have been added.

Claim Discussion – 35 U.S.C. §103

The Examiner rejected claims 13-16 under 35 USC 103(a) as being unpatentable over Sita (U.S. Patent No. 6,301,299) and Howe (U.S. Patent No. 5,900,865). Applicant respectfully disagrees with the Examiner's rejection. In particular, Sita fails to teach or suggest "storing portions of the block of data in accordance with the first and second tiled addresses such that selected portions of the block of data are *accessible at the same time* via first and second memory channels" as claimed.

In particular, as noted in the specification on page 5, lines 17-28:

> Embodiments of the present invention provide a method and apparatus for optimally mapping a tiled memory surface to two memory channels, operating in an interleaved fashion, maximizing the memory efficiency of the two channels, while maintaining the desired access granularity. In particular, an incoming request address is used to generate memory addresses for memory channels based on tile and request parameters. The memory controller stores the set of tiled data in the memory in a format such that selected set of tiled data are stored in alternating channels of memory, *such that data blocks are accessible at the same time, as opposed to sequentially*. Thus if the memory controller received a block of data from a source, such as a graphics engine, the memory controller would store portions of the block of data within a single tile in the memory, partitioned such that portions are retrievable via alternate channels of memory at the same time. (Emphasis added.)

In contrast, neither Sita or Howe, alone or in combination, teach or suggest "storing portions of the block of data in accordance with the first and second tiled addresses such that selected portions of the block of data are *accessible at the same time* via first and second memory channels" as claimed. Sita, in fact, teaches away from the claimed invention in that it specifically discloses in column 15, line 66 to column 16, line 6:

> "The exemplary embodiment of the invention uses concurrent RDRAM which allows multiple memory requests to be queued and *handled in sequence*. FIG. 6C shows an exemplary memory *sequencing* operation which performs the memory access shown in Fig. 6A. The first step in the memory sequencing shown in FIG. 6C, step 620, is a request to read a first 192 bit word from the memory operation 1 shown in FIG. 6A. "

In view of the above, all of the claims are patentable over the cited references.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

The required fee for a three month extension of time is enclosed. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, she is invited to contact the undersigned at (310) 252-7605. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on May 5, 2004.

Margaux Rodriguez *May 5, 2004*